

FEATURES

General

- Incorporates HDMI v1.4 features, including 3D video support
- 165 MHz supports all video formats up to 1080p and UXGA
- Supports gamut metadata packet transmission
- Integrated CEC buffer/controller
- Compatible with DVI v1.0 and HDCP v1.4
- Video/audio inputs accept logic levels from 1.8 V to 3.3 V

Digital video

- 3D video ready
- Programmable, 2-way color space converter
- Supports RGB, YCbCr, and DDR
- Supports ITU-656-based embedded syncs
- Automatic input video format timing detection (CEA-861-E)

Digital audio

- Supports standard S/PDIF for stereo linear pulse code modulation (LPCM) or compressed audio up to 192 kHz
- High bit rate (HBR) audio
- 8-channel uncompressed LPCM I²S audio up to 192 kHz

Special features for easy system design

- 5 V tolerant I²C and Hot Plug™ detect (HPD) I/Os, no extra device needed
- No audio master clock needed for supporting S/PDIF and I²S
- On-chip MPU with I²C master performs HDCP operations and EDID reading operations
- On-chip MPU reports HDMI events through interrupts and registers

APPLICATIONS

Gaming consoles

PCs

DVD players and recorders

Digital set-top boxes

A/V receivers

FUNCTIONAL BLOCK DIAGRAM

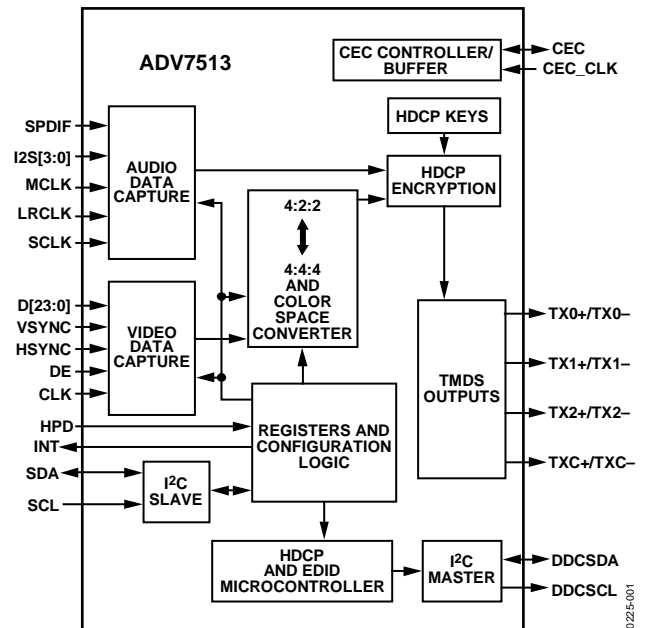


Figure 1.

GENERAL DESCRIPTION

The **ADV7513** is a 165 MHz, High-Definition Multimedia Interface (HDMI®) transmitter that is ideal for DVD players/recorders, digital set-top boxes, A/V receivers, gaming consoles, and PCs.

The digital video interface contains an HDMI v1.4/DVI v1.0-compatible transmitter and supports all HDTV formats. The **ADV7513** supports HDMI v1.4-specific features, including 3D video. The **ADV7513** also supports x.v.Color™, high bit rate (HBR) audio, and the programmable auxiliary video information (AVI) InfoFrame features. With the inclusion of HDCP, the **ADV7513** allows the secure transmission of protected content as specified by the HDCP v1.4 protocol.

The **ADV7513** supports both S/PDIF and 8-channel I²S audio. Its high fidelity 8-channel I²S interface can transmit either stereo or 7.1 surround audio up to 768 kHz. The S/PDIF interface can carry compressed audio, including Dolby® Digital, DTS®, and THX®. Fabricated in an advanced CMOS process, the **ADV7513** is provided in a 64-lead LQFP surface-mount plastic package with exposed pad and is specified over the –25°C to +85°C temperature range.

Rev. 0

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REVISION HISTORY

11/11—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

Table 1.

| Parameter | Symbol | Temp | Test Level ¹ | Min | Typ | Max | Unit |
|--|-------------------|------|-------------------------|------|------|------|-----------------|
| DIGITAL INPUTS | | | | | | | |
| Data Inputs, Video and Audio, CEC_CLK | | | | | | | |
| Input Voltage, High | V _{IH} | Full | VI | 1.35 | | 3.5 | V |
| Input Voltage, Low | V _{IL} | Full | VI | -0.3 | | +0.7 | V |
| Input Capacitance | | 25°C | VIII | | 1.0 | 1.5 | pF |
| CEC_CLK Frequency ² | | Full | VIII | 3 | 12 | 100 | MHz |
| CEC_CLK Accuracy | | Full | VIII | -2 | | +2 | % |
| DDC I²C Lines (DDCSDA, DDCSCL) | | | | | | | |
| Input Voltage, High | V _{IH} | Full | IV | 1.4 | | 5.5 | V |
| Input Voltage, Low | V _{IL} | Full | IV | -0.3 | | +0.7 | V |
| I²C Lines (SDA, SCL) | | | | | | | |
| Input Voltage, High | V _{IH} | Full | VI | 1.4 | | 5.5 | V |
| Input Voltage, Low | V _{IL} | Full | VI | -0.3 | | +0.7 | V |
| CEC Pin | | | | | | | |
| Input Voltage, High | V _{IH} | Full | VI | 2.0 | | 5.5 | V |
| Input Voltage, Low | V _{IL} | Full | VI | -0.3 | | +0.8 | V |
| Output Voltage, High | V _{OH} | Full | VI | 2.5 | | 3.63 | V |
| Output Voltage, Low | V _{OL} | Full | VI | -0.3 | | +0.6 | V |
| HPD Pin | | | | | | | |
| Input Voltage, High | V _{IH} | Full | VI | 1.3 | | 5.5 | V |
| Input Voltage, Low | V _{IL} | Full | VI | -0.3 | | +0.8 | V |
| THERMAL CHARACTERISTICS | | | | | | | |
| Thermal Resistance | | | | | | | |
| Junction-to-Case | θ _{JC} | Full | V | | 20 | | °C/W |
| Junction-to-Ambient | θ _{JA} | Full | V | | 43 | | °C/W |
| Ambient Temperature | | Full | V | -25 | +25 | +85 | °C |
| DC SPECIFICATIONS | | | | | | | |
| Input Leakage Current | I _{IL} | 25°C | VI | -1 | | +1 | μA |
| POWER SUPPLY | | | | | | | |
| 1.8 V Supply Voltage (DVDD, AVDD, PVDD, BGVDD) | | Full | IV | 1.71 | 1.8 | 1.90 | V |
| 3.3 V Supply Voltage (DVDD_3V) | | Full | IV | 3.15 | 3.3 | 3.45 | V |
| Power-Down Current | | 25°C | IV | | | 300 | μA |
| Transmitter Total Power ³ | | | | | | | |
| At 1.8 V | | Full | VI | | | 256 | mW |
| At 3.3 V | | Full | VI | | | 1 | mW |
| AC SPECIFICATIONS | | | | | | | |
| TMDS Output Clock Frequency | | 25°C | IV | 20 | | 165 | MHz |
| TMDS Output Clock Duty Cycle | | 25°C | IV | 48 | | 52 | % |
| Input Video Clock Frequency | | Full | IV | | | 165 | MHz |
| Input Video Data Setup Time ⁴ | t _{VSU} | Full | IV | 1.8 | | | ns |
| Input Video Data Hold Time ⁴ | t _{VHLD} | Full | IV | 1.3 | | | ns |
| TMDS Differential Swing | | 25°C | VII | 800 | 1100 | 1200 | mV |
| Differential Output Timing | | | | | | | |
| Low-to-High Transition Time | | 25°C | VII | 75 | 95 | | ps |
| High-to-Low Transition Time | | 25°C | VII | 75 | 95 | | ps |
| VSYNC and HSYNC Delay | | | | | | | |
| From DE Falling Edge | | 25°C | IV | | 1 | | UI ⁵ |
| To DE Rising Edge | | 25°C | IV | | 1 | | UI ⁵ |

| Parameter | Symbol | Temp | Test Level ¹ | Min | Typ | Max | Unit |
|---------------------------------|--------------------|------|-------------------------|-----|-----|-----|------|
| AUDIO AC TIMING | | | | | | | |
| SCLK Duty Cycle | | | | | | | |
| N/2 Is an Even Number | | Full | IV | 40 | 50 | 60 | % |
| N/2 Is an Odd Number | | Full | IV | 49 | 50 | 51 | % |
| I2S[3:0], S/PDIF Setup Time | t _{ASU} | Full | IV | 2 | | | ns |
| I2S[3:0], S/PDIF Hold Time | t _{AHLD} | Full | IV | 2 | | | ns |
| LRCLK Setup Time | t _{ASU} | Full | IV | 2 | | | ns |
| LRCLK Hold Time | t _{AHLD} | Full | IV | 2 | | | ns |
| I²C INTERFACE | | | | | | | |
| SCL Clock Frequency | | Full | | | | 400 | kHz |
| SDA Setup Time | t _{DSU} | Full | | 100 | | | ns |
| SDA Hold Time | t _{DHO} | Full | | 100 | | | ns |
| Setup Time for Start Condition | t _{STASU} | Full | | 0.6 | | | μs |
| Hold Time for Start Condition | t _{STAH} | Full | | 0.6 | | | μs |
| Setup Time for Stop Condition | t _{STOSU} | Full | | 0.6 | | | μs |

¹ See the Explanation of Test Levels section.

² 12 MHz crystal oscillator for default register settings.

³ 1080p, 24-bit typical random pattern.

⁴ The video data setup and hold times are measured at 0.9 V. The relationship between the clock and data is programmable in 400 ps steps.

⁵ UI is the unit interval.

ABSOLUTE MAXIMUM RATINGS

Table 2.

| Parameter | Rating |
|---|-------------------|
| Digital Inputs (SDA, SCL, DDCSDA, DDCSCL, HPD, PD) | -0.3 V to +5.5 V |
| Audio/Video Digital Inputs (D[23:0], MCLK, CLK, LRCLK, CEC, CEC_CLK, SPDIF, I2S[3:0], SCLK, HSYNC, DE, VSYNC) | -0.3 V to +3.63 V |
| Digital Output Current | 20 mA |
| Operating Temperature Range | -40°C to +100°C |
| Storage Temperature Range | -65°C to +150°C |
| Maximum Junction Temperature | 150°C |
| Maximum Case Temperature | 150°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

EXPLANATION OF TEST LEVELS

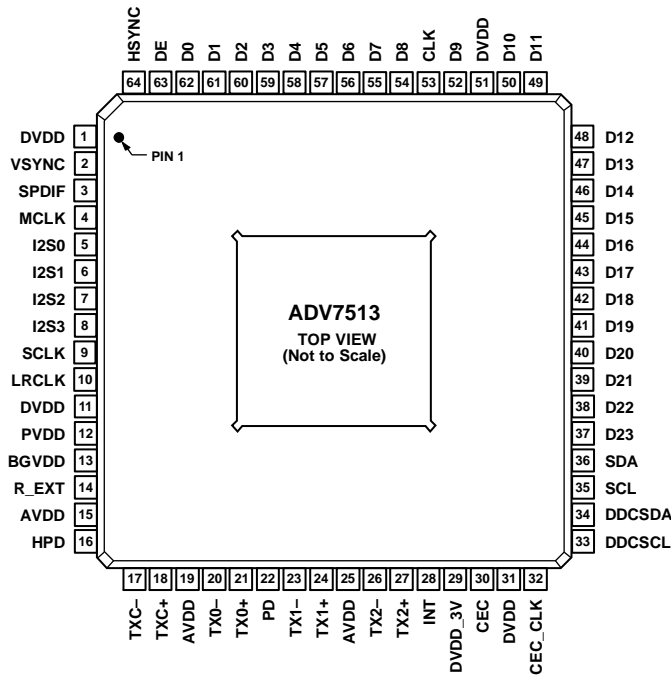
- I. 100% production tested.
- II. 100% production tested at 25°C and sample tested at specified temperatures.
- III. Sample tested only.
- IV. Parameter is guaranteed by design and characterization testing.
- V. Parameter is a typical value only.
- VI. 100% production tested at 25°C; guaranteed by design and characterization testing.
- VII. Limits defined by HDMI specification; guaranteed by design and characterization testing.
- VIII. Parameter is guaranteed by design.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
 1. THE EXPOSED PAD IS THE ELECTRICAL GROUND FOR THE PART AND MUST BE SOLDERED TO THE PCB.

Figure 2. Pin Configuration

10225-002

Table 3. Pin Function Descriptions

| Pin No. | Mnemonic | Type | Description |
|---------------|------------|---------------------|---|
| 1, 11, 31, 51 | DVDD | Power | 1.8 V Power Supply. These pins should be filtered and as quiet as possible. |
| 2 | VSYNC | Input | Vertical Synchronization Input. |
| 3 | SPDIF | Input | S/PDIF (Sony/Philips Digital Interface) Audio Input. |
| 4 | MCLK | Input | Audio Reference Clock Input. |
| 5 | I2S0 | Input | I ² S Channel 0 Audio Data Input. |
| 6 | I2S1 | Input | I ² S Channel 1 Audio Data Input. |
| 7 | I2S2 | Input | I ² S Channel 2 Audio Data Input. |
| 8 | I2S3 | Input | I ² S Channel 3 Audio Data Input. |
| 9 | SCLK | Input | I ² S Audio Clock Input. |
| 10 | LRCLK | Input | Left/Right Channel Signal Input. |
| 12 | PVDD | Power | 1.8 V PLL Power Supply. |
| 13 | BGVDD | Power | 1.8 V Band Gap Power Supply. |
| 14 | R_EXT | Input | This pin sets the internal reference currents. |
| 15, 19, 25 | AVDD | Power | 1.8 V Power Supply for TMDS Outputs. |
| 16 | HPD | Input | Hot Plug Detect Signal Input. |
| 17, 18 | TXC-, TXC+ | Differential output | Differential TMDS Clock Output. |
| 20, 21 | TX0-, TX0+ | Differential output | Differential TMDS Output Channel 0. |
| 22 | PD | Input | Power-Down Control and I ² C Address Selection. |
| 23, 24 | TX1-, TX1+ | Differential output | Differential TMDS Output Channel 1. |
| 26, 27 | TX2-, TX2+ | Differential output | Differential TMDS Output Channel 2. |

| Pin No. | Mnemonic | Type | Description |
|---------------------------|----------|--------------|--|
| 28 | INT | Output | Interrupt Signal Output. |
| 29 | DVDD_3V | Power | 3.3 V Power Supply. |
| 30 | CEC | Input/output | CEC Data Signal. |
| 32 | CEC_CLK | Input | CEC Clock (Oscillator from 3 MHz to 100 MHz). |
| 33 | DDCSCL | Control | Serial Port Data Clock to Sink. |
| 34 | DDCSDA | Control | Serial Port Data Input/Output to Sink. |
| 35 | SCL | Control | Serial Port Data Clock Input. |
| 36 | SDA | Control | Serial Port Data Input/Output. |
| 37 to 50, 52, 54 to 62 | D[23:0] | Input | Video Data Inputs. |
| 53 | CLK | Input | Video Input Clock. |
| 63 | DE | Input | Data Enable Signal for Digital Video. |
| 64 | HSYNC | Input | Horizontal Synchronization Input. |
| | EPAD | Power | The exposed pad is the electrical ground for the part and must be soldered to the PCB. |

APPLICATIONS INFORMATION

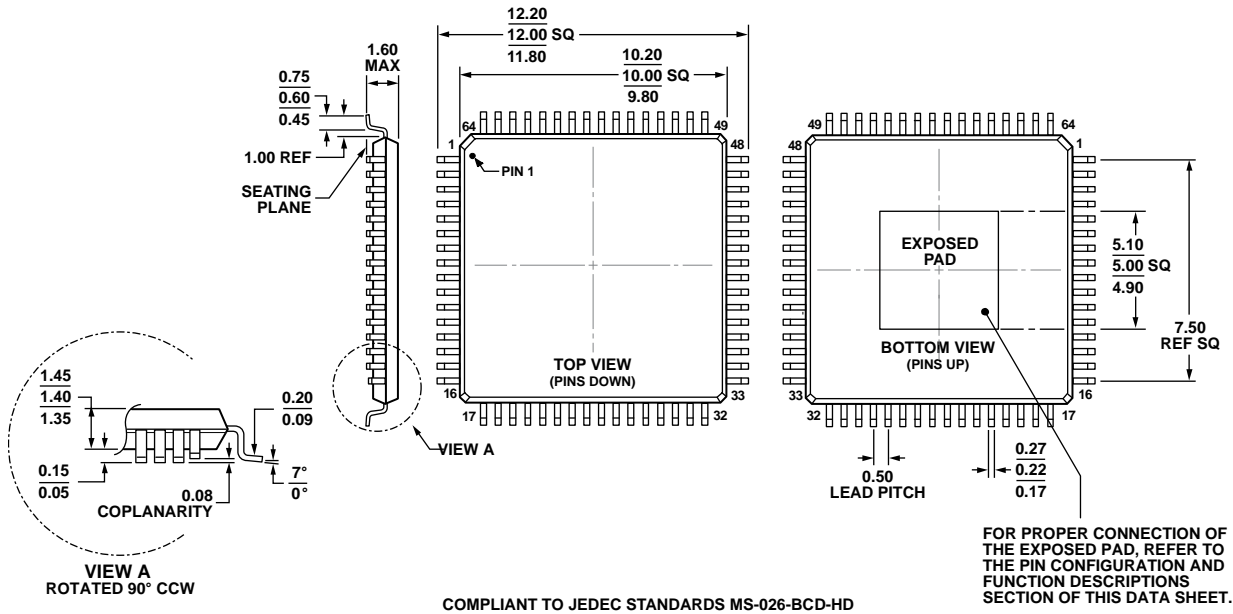
DESIGN RESOURCES

Evaluation kits, reference design schematics, hardware and software guides, and other support documentation are available under a nondisclosure agreement (NDA). For more information, contact ATV_VideoTx_Apps@analog.com.

Other references include the following:

- *EIA/CEA-861-E*—this technical specification document describes audio and video InfoFrames, as well as the E-EDID structure for HDMI. It is available from the Consumer Electronics Association (CEA).
- *High-Definition Multimedia Interface Specification Version 1.4*, a defining document for HDMI v1.4, and the *HDMI Compliance Test Specification (CTS) Version 1.3a* are available from HDMI Licensing, LLC.
- *High-Bandwidth Digital Content Protection System Revision 1.4*, the defining technical specification document for HDCP Revision 1.4, is available from Digital Content Protection, LLC.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-BCD-HD
 Figure 3. 64-Lead Low Profile Quad Flat Package [LQFP_EP]
 (SW-64-2)
 Dimensions shown in millimeters

ORDERING GUIDE

| Model ¹ | Temperature Range | Package Description | Package Option |
|--------------------|-------------------|--|----------------|
| ADV7513BSWZ | -25°C to +85°C | 64-Lead Low Profile Quad Flat Package, Exposed Pad [LQFP_EP] | SW-64-2 |
| EVAL-ADV7513-AKZ | | Evaluation kit with HDCP keys | |

¹ Z = RoHS Compliant Part.

NOTES

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NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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